In the Specification:

Please replace the paragraph beginning on page 1, line 7, with the following rewritten paragraph:

--The present invention relates to the field of so-called flip-chip packaging. Flip chip technology is well known in the art of semiconductor packaging, and detailed information concerning flip chip packaging may be found in references such as Microchip Fabrication (3rd Ed.) by Van Zant, P., Chapter 18 "Packaging" (1997) and Ball Grid Array Technology, edited by Lau, John H. (1995), which are hereby incorporated by reference. Some methods of flip-chip packaging use packaging substrates which include one or more bonding pads on one of the substrate surfaces. These bonding pads have a number of circuit connections which will be contacted to a semiconductor chip (or "die"). The die features a plurality of leads which are used to interconnect the die to the packaging substrate. In order to efficiently connect the die to the bonding pad, the leads of the die are treated with tiny lumps of solder ("bumps"), which are used to interconnect the die to other circuit elements, including a bonding pad. Ordinarily, the dies are attached by dipping the die in flux such that the bump surfaces are covered in a small amount of flux. The flux treated die is then carefully aligned and placed on the bonding pads of the packaging substrate. The packaging substrate and die are then placed in a reflow furnace, where the packaging substrate and die are subjected to a carefully controlled temperature process designed to optimize the bond between the bumps and the bonding pad. This process of heating the bumps to a desired melting temperature to

electrically connect the die to the packaging substrate is known as reflowing. Once this reflow process is completed, the packaging substrates and their newly bonded dies are subjected to further processing as needed.--

Please replace the paragraph beginning on page 2, line 5, with the following rewritten paragraph:

--To create a good contact between the die and the bonding pad, the process temperatures must be carefully controlled. A typical attachment process begins by aligning the die to the substrate and tacking it in place with flux. Then the die and packaging substrate are placed in a reflow furnace. For example, multizone reflow furnaces may be used to heat the die and package to the required temperatures. In the first zone the die and package are typically preheated to a baseline preheating temperature. Once preheated, the substrate and die are passed into a melt zone, typically maintained at a higher temperature. There the substrate and die are then subjected to a melt temperature which melts the solder bumps creating the bond between the bonding pad and the die. Once this is accomplished, the die and substrate are passed onto a cool down zone of the furnace, which allows the solder to cool without degrading the bond between the die and bonding pad. The temperature of each zone is largely dependent on the type of solder used to form the bumps. Each of these three steps (preheat, melt, and cool down) are very temperature critical requiring accurate thermal calibration of each zone. In the past, these temperatures were calibrated by a process known as thermal profiling. Thermal profiling is used to monitor a temperature vs. time curve. Although the

reflow furnaces themselves are set at a certain temperature, this is not the same as the temperature at the interface between the die and the bonding pad. Since it is the interface temperature that is critical, more accurate measurements of the interface temperature are required. Previously, thermal profiling had been done by placing a die on a packaging substrate, then attaching a thermocouple on top of the die and running the substrate through a preheat, melt, cool down cycle in a reflow furnace. The furnace temperatures were then adjusted until the optimum preheat, melt, and cool down temperatures were measured by the thermocouple.--

A 2 cont.

Please replace the paragraph beginning on page 2, line 28, with the following rewritten paragraph:

A 3

--The inventors have discovered that using these methods does not accurately profile the temperature at the interface between the die and the bonding pad. The inventors have discovered that the temperatures of the previously used methods can vary as much as 10° C from the actual interface temperature. This leads to sub-optimal bonding of the die to the bonding pad. This increases chip failure rate and reduces chip reliability, and is therefore undesirable.--

In the Claims:

Please Cancel Claim 7 without prejudice or disclaimer.

Please cancel Claims 8-11 without prejudice or disclaimer subject to the restriction requirement.